IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A method for identifying potential noise failures in an integrated circuit design comprising:

locating a victim net and an aggressor within the integrated circuit design;

modeling the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor; and

indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

2. (Original) The method defined in Claim 1 wherein modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location.

3. (Original) The method defined in Claim 1 wherein modeling the victim net comprises determining noise width.

4. (Previously Presented) The method defined in Claim ~~3~~ 6 wherein the noise

width is determined corresponding to:

$$t_v \ln\left[\frac{(t_x - t_r v_t)\left(e^{t_r/t_v} - 1\right)}{t_r v_t}\right]$$

where t_r comprises transition time, t_v comprises distributed Elmore delay of the victim net, t_x comprises the RC delay term from the upstream resistance of the coupling elements multiplied by the coupling capacitance, and v_t comprises a threshold voltage.

5. (Original) The method defined in Claim 4 wherein the threshold voltage is set to half of the peak noise voltage.

6. (Previously Presented) A method for identifying potential noise failures in an integrated circuit design comprising:

locating a victim net and an aggressor within the integrated circuit design;

modeling the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and determining noise width, wherein the noise width is determined corresponding to:

$$t_r + t_v \ln\left[\frac{1 - e^{-2t_r/t_v}}{1 - e^{-t_r/t_v}}\right]$$

where t_r comprises transition time and t_v comprises a distributed Elemore delays of the victim net; and

indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

7. (Previously Presented) A method for identifying potential noise failures in an integrated circuit design comprising:

locating a victim net and an aggressor within the integrated circuit design;

modeling the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and determining noise width, wherein the noise width is based on only transition time and distributed Elmore delay of the victim net; and

indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

8. (Previously Presented) A method for identifying potential noise failures in an integrated circuit design comprising:

locating a victim net and an aggressor within the integrated circuit design;

modeling the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and determining noise width, wherein the noise width is independent of an RC delay term from upstream resistance of the coupling element times coupling capacitance of the coupling location; and

indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

9. (Original) The method defined in Claim 1 wherein modeling the victim net comprises determining the peak noise amplitude.

10. (Previously Presented) The method defined in Claim 9 wherein the peak noise amplitude is determined according to:

$$\frac{(R_d + R_s)C_x}{R_d(C_1 + C_x + C_2 + C_L) + R_s(C_x + C_2 + C_L) + R_e C_L}$$

where R_d comprises the effective resistance of the victim driver, R_s comprises the upstream wire resistance from the victim driver to the coupling center, R_e is the downstream wire resistance from the coupling center to the receiver under noise consideration, C_x is the coupling capacitance, C_1 is half of the upstream wiring capacitance from the coupling center to the driver, C_2 is half of the total wire capacitance on the path from the driver to the receiver, and C_L is half of the total wire capacitance from the coupling center to the receiver, plus the receiver input capacitance.

11. (Original) The method defined in Claim 1 wherein modeling the victim net comprises computing crosstalk noise at a sink with a lumped capacitance at each branch incorporated on a path from a source to the sink, with lumped

capacitances being added in a weighted manner based on their locations on the path.

12. (Original) An article of manufacture comprising one or more recordable medium having executable instructions stored thereon which, when executed by a system, cause the system to:

locate a victim net and an aggressor within the integrated circuit design;

model the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor; and

indicate that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

13. (Original) The article of manufacture defined in Claim 12 further comprising instructions to model the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location.

14. (Original) The article of manufacture defined in Claim 12 wherein instructions to model the victim net comprise instructions to determine noise width.

15. (Previously Presented) The article of manufacture defined in Claim 17 ~~14~~ wherein the noise width is determined corresponding to:

$$t_v \ln\left[\frac{(t_x - t_r v_t)(e^{t_r/t_v} - 1)}{t_r v_t}\right]$$

where t_r comprises transition time, t_v comprises distributed Elmore delay of the victim net, t_x comprises the RC delay term from the upstream resistance of the coupling elements multiplied by the coupling capacitance, and v_t comprises a threshold voltage.

16. (Original) The article of manufacture defined in Claim 15 wherein the threshold voltage is set to half of the peak noise voltage.

17. (Currently Amended) An article of manufacture comprising one or more recordable medium having executable instructions stored thereon which, when executed by a system, cause the system to:

locate a victim net and an aggressor within the integrated circuit design;

model the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and ~~instructions~~ to determine noise width, wherein the noise width is determined corresponding to:

$$t_r + t_v \ln\left[\frac{1 - e^{-2t_r/t_v}}{1 - e^{-t_r/t_v}}\right]$$

where t_r comprises transition time and t_v comprises a distributed Elemore delays of the victim net; and

indicate that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

18. (Currently Amended) An article of manufacture comprising one or more recordable medium having executable instructions stored thereon which, when executed by a system, cause the system to:

locate a victim net and an aggressor within the integrated circuit design;

model the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and ~~instructions~~ to determine noise width, wherein the noise width is based on only transition time and distributed Elmore delay of the victim net; and

indicate that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

19. (Currently Amended) An article of manufacture comprising one or more recordable medium having executable instructions stored thereon which, when executed by a system, cause the system to:

locate a victim net and an aggressor within the integrated circuit design;

model the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and

~~instructions~~ to determine noise width, wherein the noise width is independent of an RC delay term from upstream resistance of the coupling element times coupling capacitance of the coupling location; and

indicate that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

20. (Original) The article of manufacture defined in Claim 12 wherein instructions to model the victim net comprise instructions to determine the peak noise amplitude.

21. (Previously Presented) The article of manufacture defined in Claim 20 wherein the peak noise amplitude is determined according to:

$$\frac{(R_d + R_s)C_x}{R_d(C_1 + C_x + C_2 + C_L) + R_s(C_x + C_2 + C_L) + R_e C_L}$$

where R_d comprises the effective resistance of the victim driver, R_s comprises the upstream wire resistance from the victim driver to the coupling center, R_e is the downstream wire resistance from the coupling center to the receiver under noise consideration, C_x is the coupling capacitance, C_1 is half of the upstream wiring capacitance from the coupling center to the driver, C_2 is half of the total wire capacitance on the path from the driver to the receiver, and C_L is half of the total wire capacitance from the coupling center to the receiver, plus the receiver input capacitance.

22. (Original) The article of manufacture defined in Claim 12 wherein instructions to model the victim net comprise instructions to compute crosstalk noise at a sink with a lumped capacitance at each branch incorporated on a path from a source to the sink, with lumped capacitances being added in a weighted manner based on their locations on the path.

23. (Original) An apparatus for identifying potential noise failures in an integrated circuit design comprising:

means for locating a victim net and an aggressor within the integrated circuit design;

means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor; and

means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

24. (Original) The apparatus defined in Claim 23 wherein the means for modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises means for modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location.

25. (Original) The apparatus defined in Claim 23 wherein the means for modeling the victim net comprises means for determining noise width.

26. (Previously Presented) The apparatus defined in Claim 25 wherein the noise width is determined corresponding to:

$$t_v \ln\left[\frac{(t_x - t_r v_t)(e^{t_r/t_v} - 1)}{t_r v_t}\right]$$

where t_r comprises transition time, t_v comprises distributed Elmore delay of the victim net, t_x comprises the RC delay term from the upstream resistance of the coupling elements multiplied by the coupling capacitance, and v_t comprises a threshold voltage.

27. (Original) The apparatus defined in Claim 26 wherein the threshold voltage is set to half of the peak noise voltage.

28. (Previously Presented) An apparatus for identifying potential noise failures in an integrated circuit design comprising:

means for locating a victim net and an aggressor within the integrated circuit design;

means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the

aggressor and means for determining noise width, wherein the noise width is determined corresponding to:

$$t_r + t_v \ln\left[\frac{1-e^{-2t_r/t_v}}{1-e^{-t_r/t_v}}\right]$$

where t_r comprises transition time and t_v comprises a distributed Elemore delays of the victim net; and

means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

29. (Previously Presented) An apparatus for identifying potential noise failures in an integrated circuit design comprising:

means for locating a victim net and an aggressor within the integrated circuit design;

means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor and means for determining noise width, wherein the noise width is based on only transition time and distributed Elmore delay of the victim net; and

means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

30. (Previously Presented) An apparatus for identifying potential noise failures in an integrated circuit design comprising:

means for locating a victim net and an aggressor within the integrated circuit design;

means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor and means for determining noise width, wherein the noise width is independent of an RC delay term from upstream resistance of the coupling element times coupling capacitance of the coupling location; and

means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.

31. (Original) The apparatus defined in Claim 23 wherein the means for modeling the victim net comprises means for determining the peak noise amplitude.

32. (Previously Presented) The apparatus defined in Claim 31 wherein the peak noise amplitude is determined according to:

$$\frac{(R_d + R_s)C_x}{R_d(C_1 + C_x + C_2 + C_L) + R_s(C_x + C_2 + C_L) + R_e C_L}$$

where R_d comprises the effective resistance of the victim driver, R_s comprises the upstream wire resistance from the victim driver to the coupling center, R_e is the downstream wire resistance from the coupling center to the receiver under noise

consideration, C_x is the coupling capacitance, C_1 is half of the upstream wiring capacitance from the coupling center to the driver, C_2 is half of the total wire capacitance on the path from the driver to the receiver, and C_L is half of the total wire capacitance from the coupling center to the receiver, plus the receiver input capacitance.

33. (Original) The apparatus defined in Claim 23 wherein the means for modeling the victim net comprises computing crosstalk noise at a sink with a lumped capacitance at each branch incorporated on a path from a source to the sink, with lumped capacitances being added in a weighted manner based on their locations on the path.